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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Hiroshi MAKAMURA, et al.

PATENT NO.: 7,301,834

GROUP: 2824

ISSUED: November 27, 2007

EXAMINER: NGUYEN, NAM THANH

FOR: SEMICONDUCTOR MEMORY

REQUEST FOR CERTIFICATE OF CORRECTION

DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE ALEXANDRIA, VA 22313-1450

SIR:

The following is a Request for Certificate of Correction in Serial Number 10/694,861, now U.S. Patent Number 7,301,834.

In accordance with the provisions of Rule 322 of the Rules of Practice, which implement 35 USC 254, the U.S. Patent and Trademark Office is respectfully requested to issue a Certificate of Correction in the above-identified patent.

In light of the fact that the errors were the fault of the U.S. Patent and Trademark Office, no fees are required. The requested corrections are listed on FORM P.T.O. 1050.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,

MAIER & NEUSTADT, P.C.

Marvin J. Spivak

Registration No. 24,913

Customer Number

22850

Tel. (703) 413-3000 Fax. (703) 413-2220 (OSMMN 03/06) Paul J. Killos Registration No. 58,014 UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.:

7,301,834

DATED:

November 27, 2007

INVENTOR(S):

Hiroshi MAKAMURA, et al.

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, Item (75), the Inventors information is incorrect. Item (75) should read:

-- (75) Inventors: **Hiroshi Makamura,** Fujisawa (JP); **Toshio Yamamura,** Yokohama (JP) --

Mailing address of sender:

Patent No.

7,301,834

Customer Number

No. of add'l copies @ .30 per page

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Tel. (703) 413-3000 Fax. (703) 413-2220 (OSMMN 03/06)